

CHIPLINK P-Channel Enhancement Mode Power MOSFET

Description

The LX30P50N combines advanced trench technology to provide excellent $R_{DS(ON)}$, it tailored to minimize conduction loss, and provide superior switching performance.

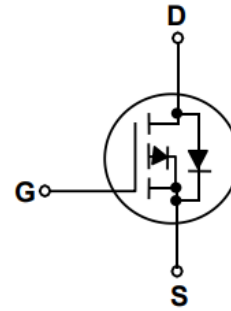
Features

- $V_{DS}=-30V$, $I_D=-50A$
 $R_{DS(ON)typ.}=8.6m\Omega@V_{GS}=-10V$
 $R_{DS(ON)typ.}=11.5m\Omega@V_{GS}=-4.5V$
- Fast switching
- High power and current handing capability
- Termination is Lead-free and RoHS Compliant

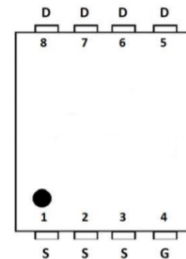


Applications

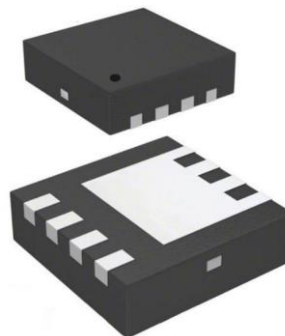
- PWM applications
- Load switch
- Power Management



Schematic Diagram



Pin Assignment



DFN3*3 Package

Maximum Ratings($T_A=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	$I_D(T_C=25^{\circ}C)$	-50	A
	$I_D(T_C=100^{\circ}C)$	-33	
Pulsed Drain Current ^B	I_{DM}	-200	A
Maximum Power Dissipation ^A	P_D	20	W
Single pulse avalanche energy	E_{AS}	225	mJ
Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^{\circ}C$

Thermal Characteristic

Thermal Resistance, Junction to Case	R_{QJC}	6.25	$^{\circ}\text{C/W}$
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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Test conditions	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250uA	-30			V
Gate-Threshold Voltage	V _{th(GS)}	V _{DS} = V _{GS} , I _D =-250 uA	-1	-1.5	-2.0	V
Gate-body Leakage	IGSS	V _{DS} =0V, V _{GS} =±12V			±100	nA
Zero Gate Voltage Drain Current	IDSS	V _{DS} =-30V, V _{GS} =0V			-1	uA
Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-12A		8.6	12	mΩ
		V _{GS} =-4.5V, I _D =-7A		11.5	17	mΩ
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} = -15V, V _{GS} =0V, F=1MHz		1770		pF
Output Capacitance	C _{oss}			231		
Reverse Transfer Capacitance	C _{rss}			215		
Switching Capacitance						
Turn-on Delay Time	t _{d(on)}	V _{DD} = -15V, R _L =3Ω V _{GS} = -10V, R _{GEN} =3Ω		13		nS
Turn-on Rise Time	t _r			8.5		nS
Turn-off Delay Time	t _{d(off)}			26		nS
Turn-off Fall Time	t _f			12		nS
Total Gate Charge	Q _g	V _{DS} = -15V, I _D =-25A, V _{GS} =-10V		32		nC
Gate-Source Charge	Q _{gs}			6		nC
Gate-Drain Charge	Q _{gd}			10		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _D =-10A			-1.2	V
Diode Forward Current	I _s				-50	A

Notes:

- The Power dissipation P_D is based on $T_{J(MAX)}=150^{\circ}\text{C}$, using $\leq 10s$ junction-to ambient thermal resistance.
- Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^{\circ}\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^{\circ}\text{C}$.
- The Static characteristics in Figures are obtained using $<300\mu s$ pulses, duty cycle 2% max.
- EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=-25V, V_{GS}=-10V, L=0.5Mh$.

Typical Electrical and Thermal Characteristics

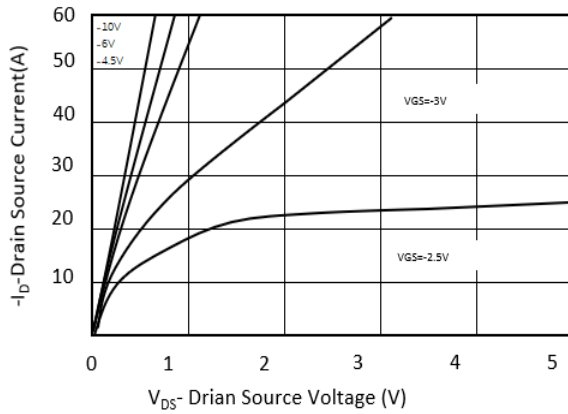


Figure 1: On-Region Characteristics

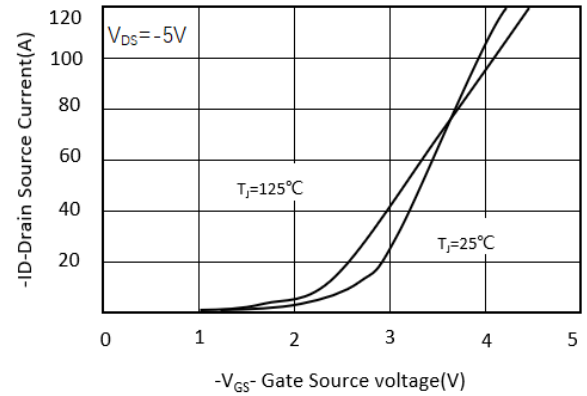


Figure 2: Transfer Characteristics

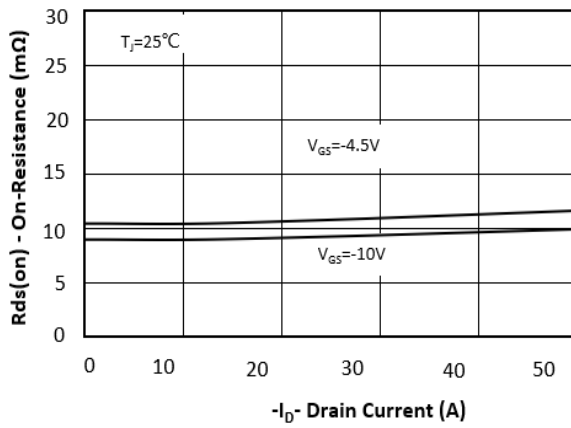


Figure 3: On-resistance vs. Drain Current

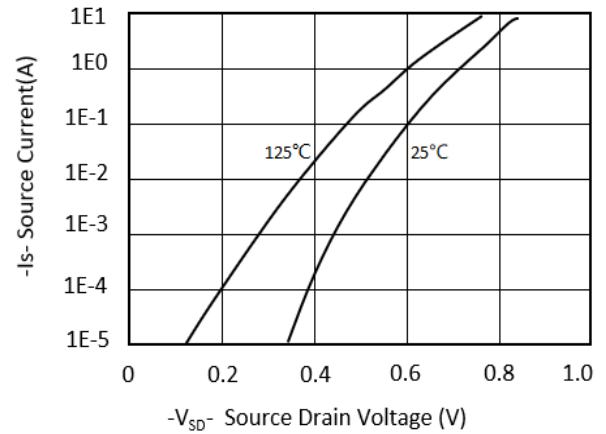


Figure 4: Body Diode Characteristics

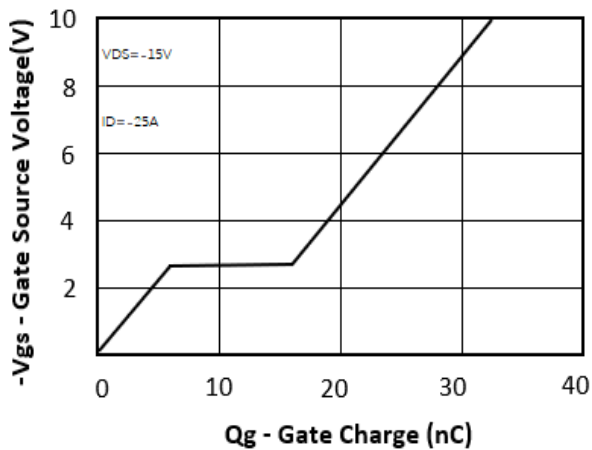


Figure 5: Gate Charge Characteristics

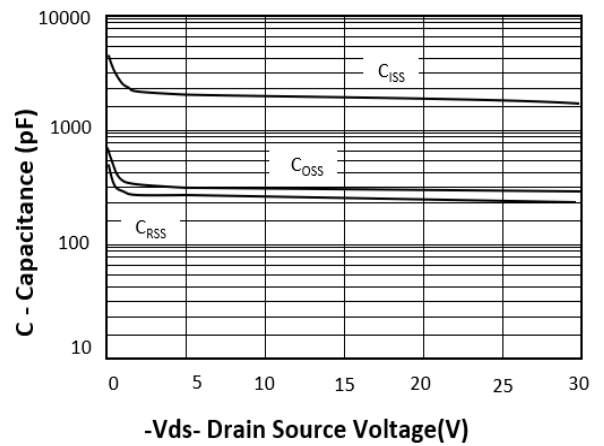


Figure 6: Capacitance Characteristics

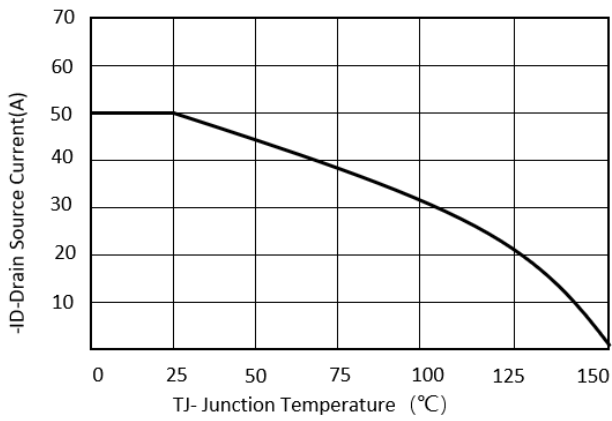


Figure 7: Current De-rating

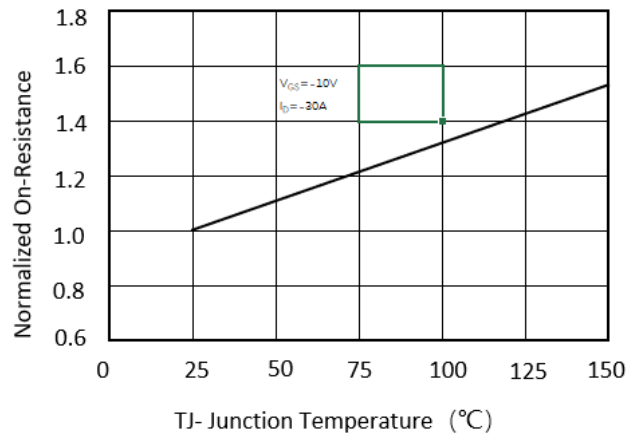


Figure 8: On-Resistance Vs. Junction Temperature

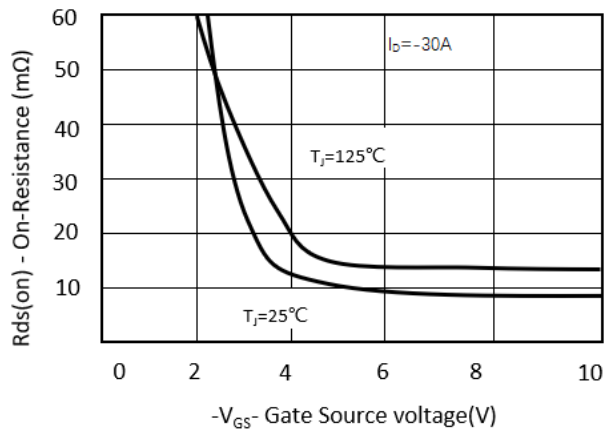


Figure 9: On-Resistance Vs. Gate-Source Voltage

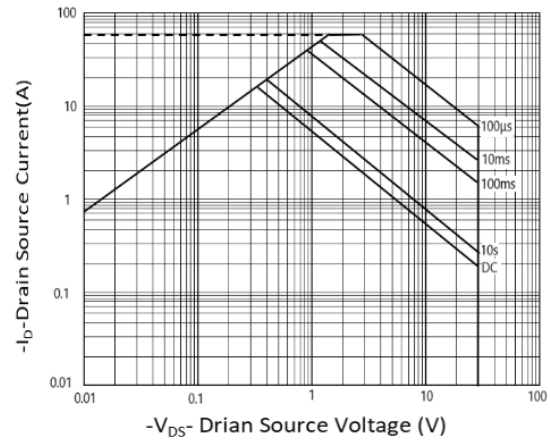


Figure 10: Safe Operation Area

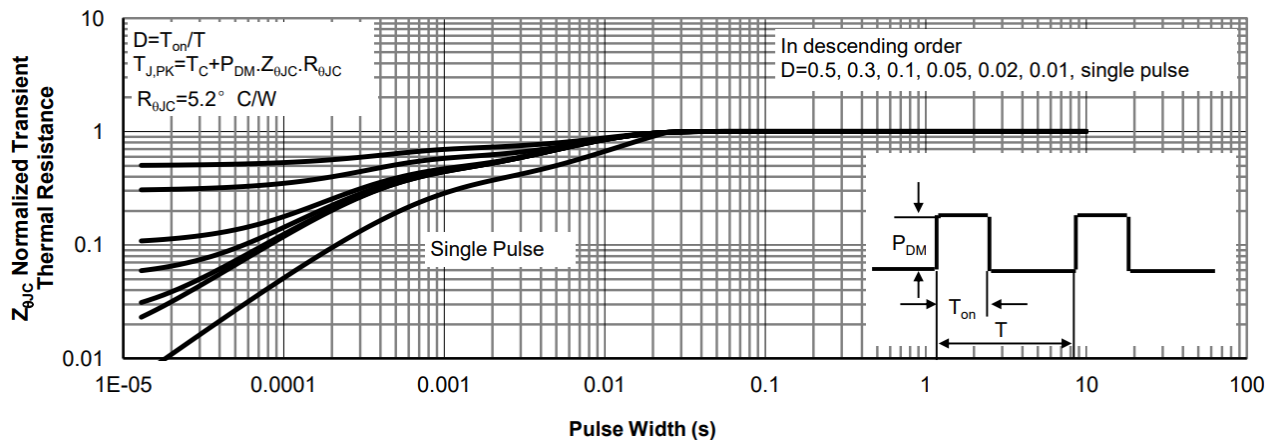
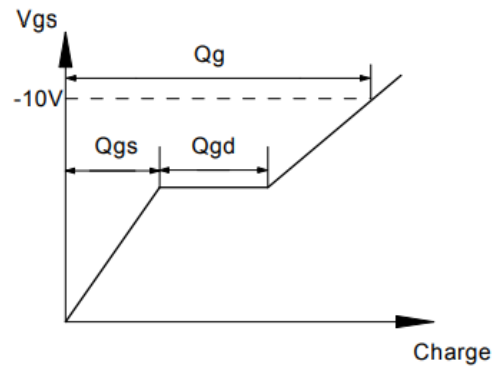
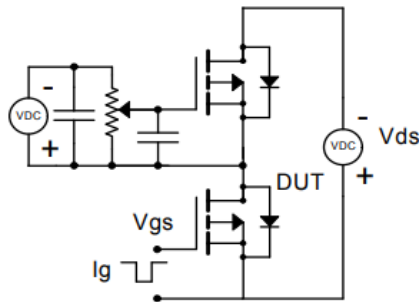
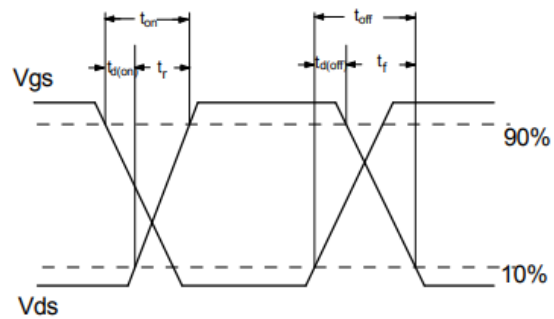
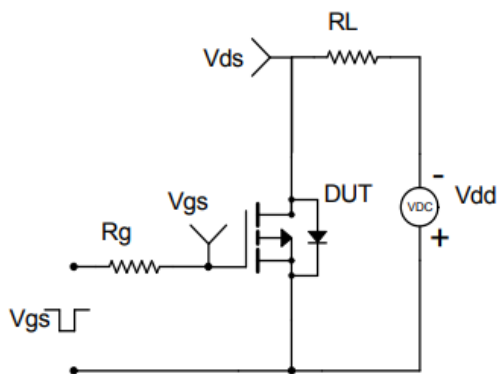


Figure 11: Normalized Maximum Transient Thermal Impedance

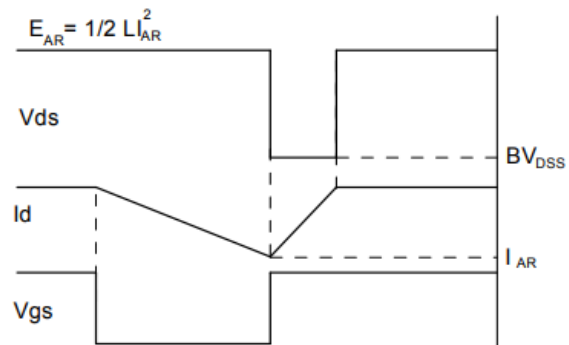
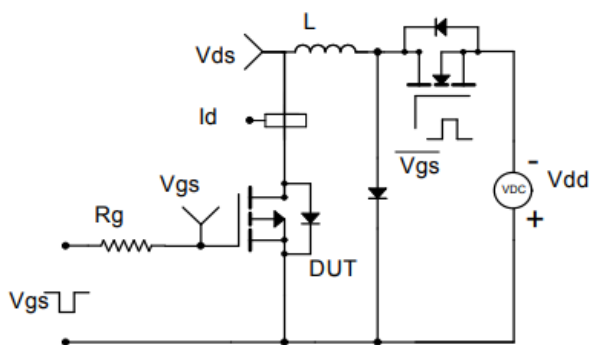
Gate Charge Test Circuit & Waveform



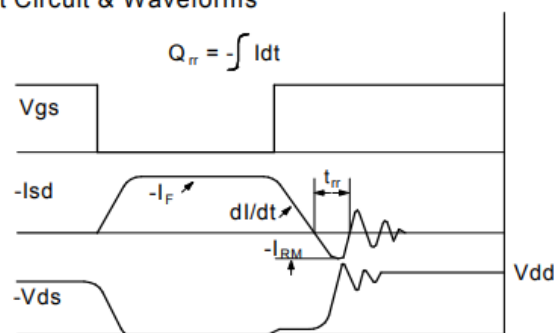
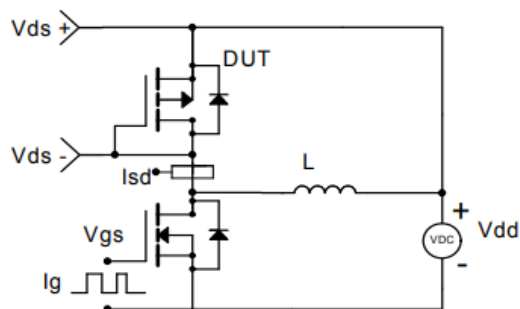
Resistive Switching Test Circuit & Waveforms



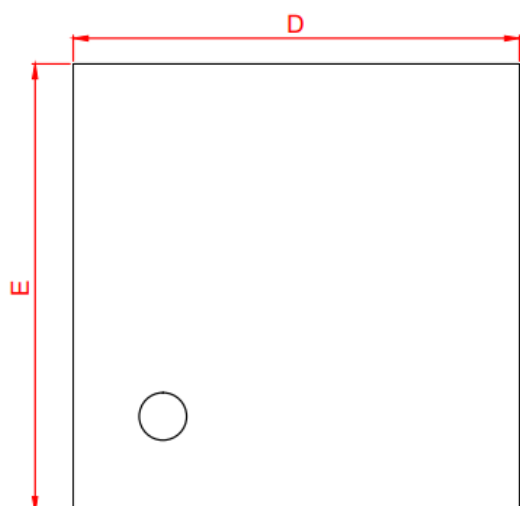
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



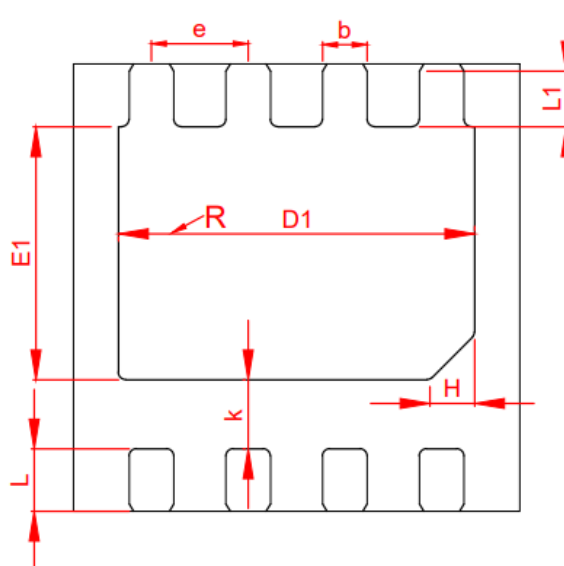
Diode Recovery Test Circuit & Waveforms



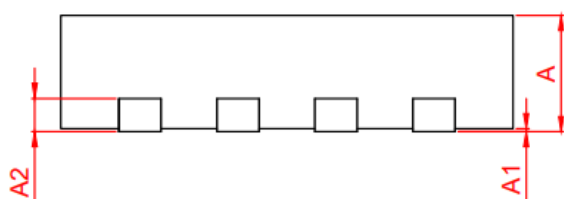
DFN3*3 Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
* A1	0.00	0.02	0.05
* b	0.27	0.32	0.37
* A2	0.20REF		
* D	2.90	3.00	3.10
* E	2.90	3.00	3.10
* E1	1.70	1.80	1.90
* D1	2.35	2.45	2.55
* e	0.65BSC		
* L	0.35	0.40	0.45
h	0.30 REF		
* k	0.50REF		
* L1	0.25	0.30	0.35

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