CHIPLINK P-Channel Enhancement Mode Power MOSFET

Description

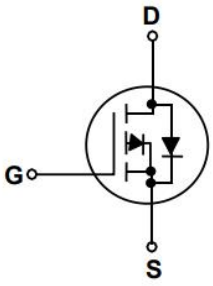
The LX30P30N combines advanced trench technology to provide excellent $R_{DS(ON)}$, it is tailored to minimize conduction loss, and provide superior switching performance.

Features

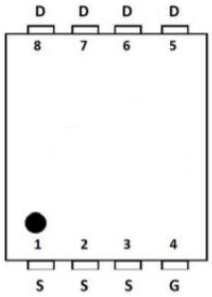
- V_{DS}=-30V, I_D=-30A
  $R_{DS(ON)typ.}$ =10.5mΩ@V_{GS}=-10V
  $R_{DS(ON)typ.}$ =15mΩ@V_{GS}=-4.5V
- Fast Switching
- High Power and Current Handing Capability
- Termination is Lead-Free and RoHS Compliant

Applications

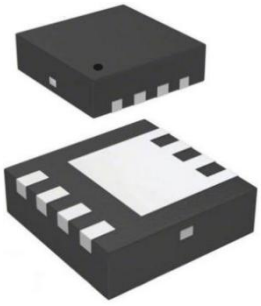
- PWM Applications
- Load Switch
- Power Management



Schematic Diagram



Pin Assignment



PDFN3*3 Package

Maximum Ratings

(T_A=25℃ unless otherwise noted)

PARAMETER	SYMBOL	MAX	UNIT
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	I_D (T_C = 25℃)	-30	A
	I_D (T_C = 100℃)	-20	A
Pulsed Drain Current [B]	I_{DM}	-120	A
Maximum Power Dissipation [A]	P_D	16	W
Single Pulse Avalanche Energy	E_{AS}	180	mJ
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	℃

Thermal Characteristic

Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	℃/W

Electrical Characteristics

(T_A=25℃ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-30			V
Gate-Threshold Voltage	$V_{th(GS)}$	V_{DS} = V_{GS}, I_D = -250μA	-1	-1.5	-2	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -30V, V_{GS} = 0V			-1	μA
Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS} = -10V, I_D = -6A		10.5	14	mΩ
		V_{GS} = -4.5V, I_D = -5A		15	19	mΩ
Dynamic Characteristics						
Input Capacitance	C_{iss}	V_{DS} = -15V, V_{GS} = 0V, F = 1MHz		1582		pF
Output Capacitance	C_{oss}			198		
Reverse Transfer Capacitance	C_{rss}			173		
Switching Capacitance						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -15V, R_L= 3Ω V_{GS} = -10V, R_{GEN} = 3Ω		13		ns
Turn-On Rise Time	t_r			8.5		ns
Turn-Off Delay Time	$t_{d(off)}$			26		ns
Turn-Off Fall Time	t_f			12		ns
Total Gate Charge	Q_g	V_{DS} = -15V, I_D = -15A, V_{GS} = -10V		29		nC
Gate-Source Charge	Q_{gs}			5		nC
Gate-Drain Charge	Q_{gd}			8		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS} = 0V, I_D = -10A			-1.2	V
Diode Forward Current	I_S				-30	A

Notes:

A. The Power dissipation P_D is based on $T_{J(MAX)}$=150℃, using≤10s junction-to-ambient thermal resistance.

B. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150℃. Ratings are based on low frequency and duty cycles to keep initial T_J=25℃.

C. The Static characteristics in Figures are obtained using<300μs pulses, duty cycle 2% max.

D. E_{AS} condition: T_J=25℃, V_{DD}=-25V, V_{GS}=-10V, L=0.5mH.

Typical Electrical and Thermal Characteristics

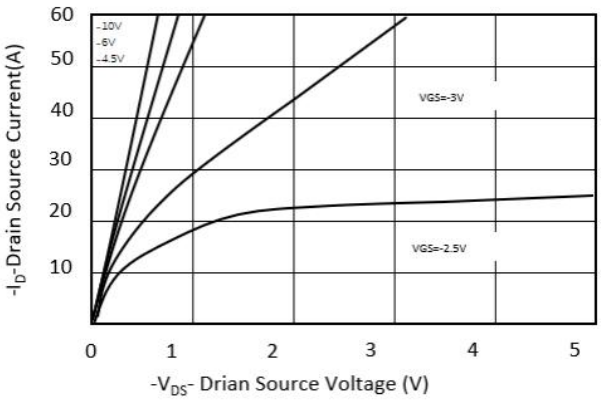


Figure 1. On-Region Characteristics

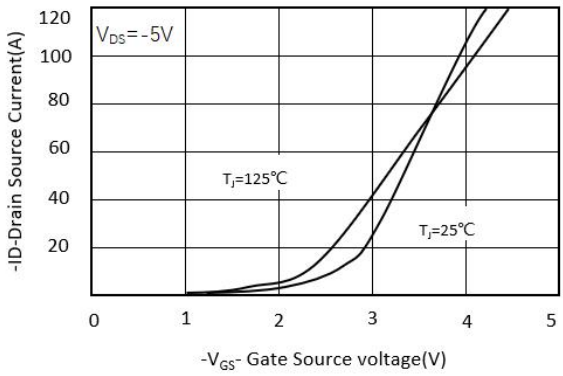


Figure 2. Transfer Characteristics

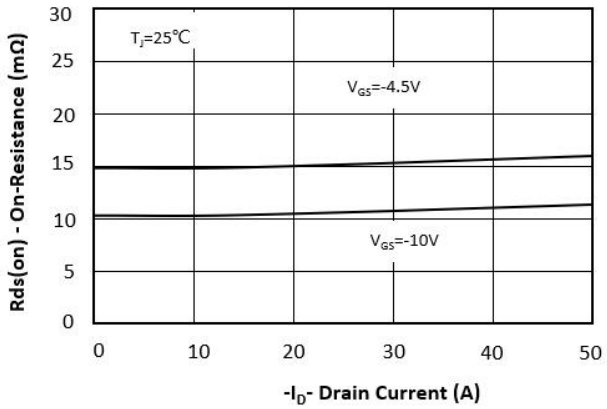


Figure 3. On-Resistance vs. Drain Current

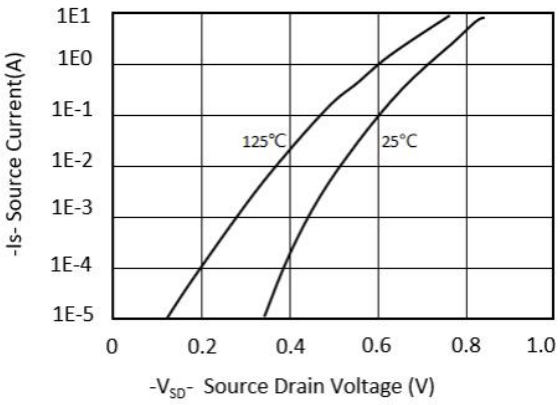


Figure 4. Body Diode Characteristics

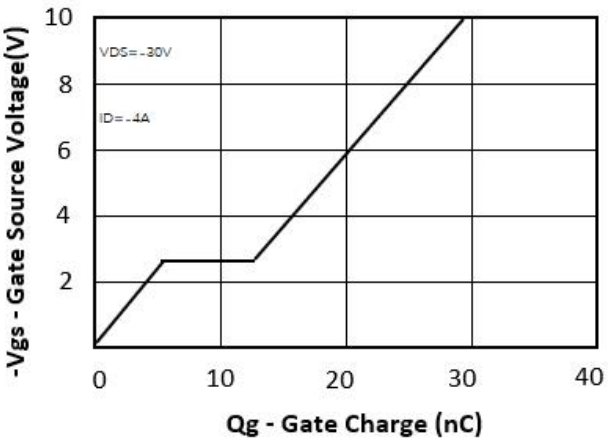


Figure 5. Gate Charge Characteristics

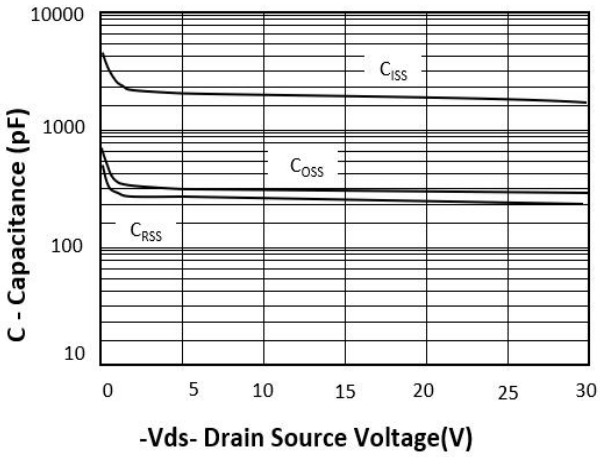


Figure 6. Capacitance Characteristics

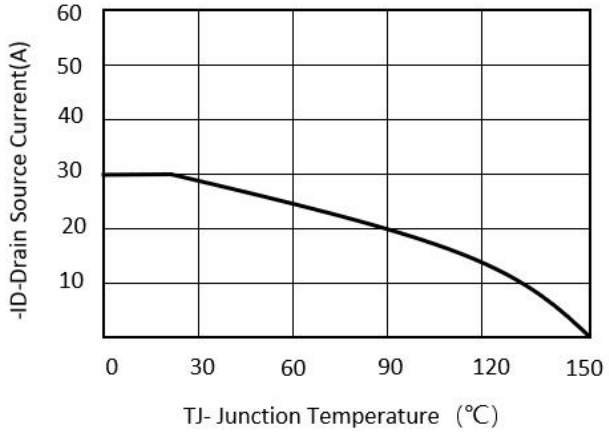


Figure 7. Current De-rating

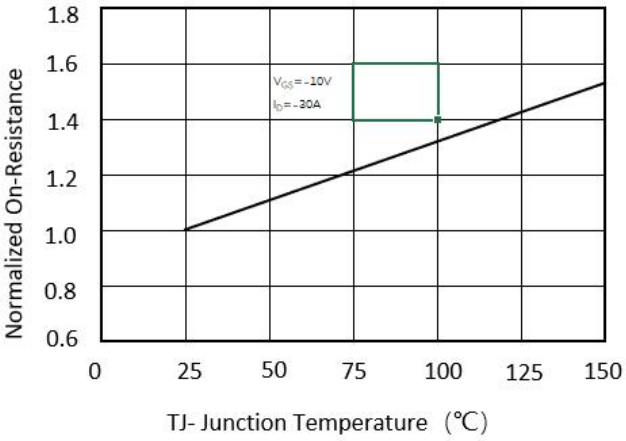


Figure 8. On-Resistance vs. Junction Temperature

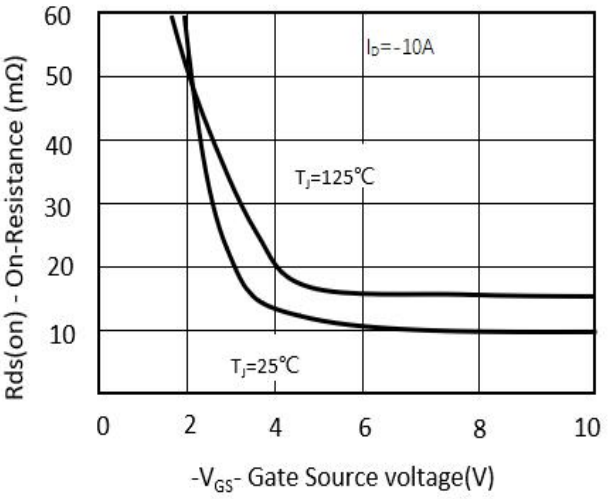


Figure 9. On-Resistance vs. Gate-Source Voltage

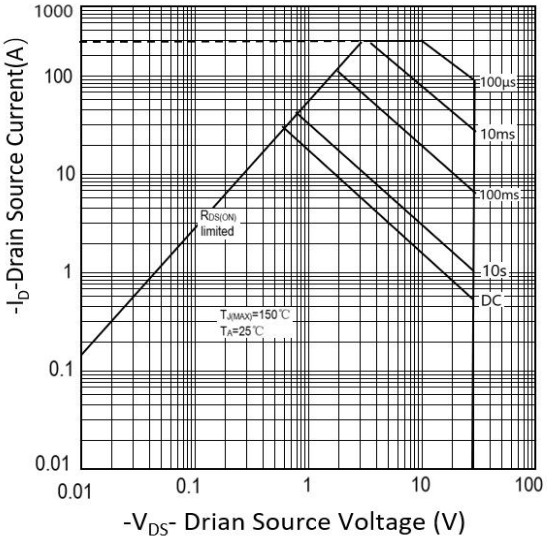


Figure 10. Safe Operation Area

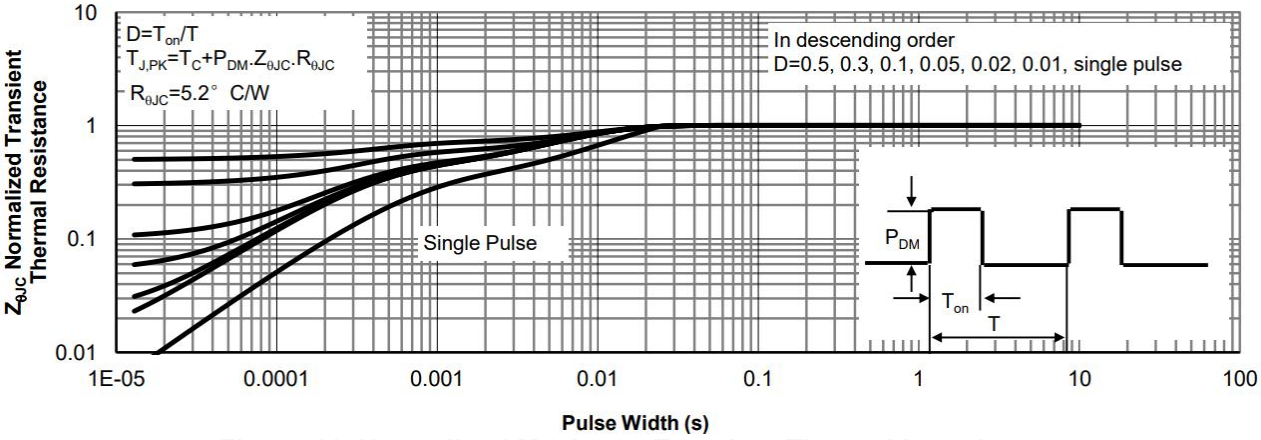


Figure 11. Normalized Maximum Transient Thermal Impedance

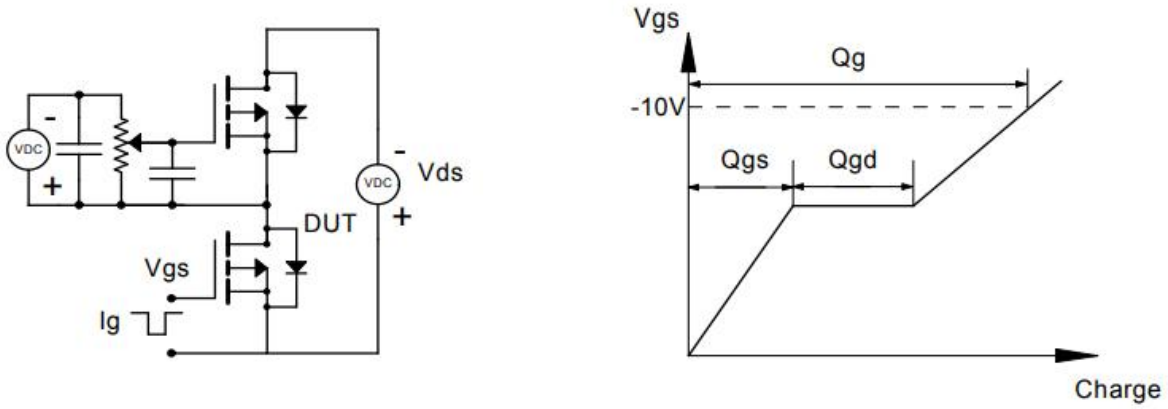


Figure 12. Gate Charge Test Circuit & Waveform

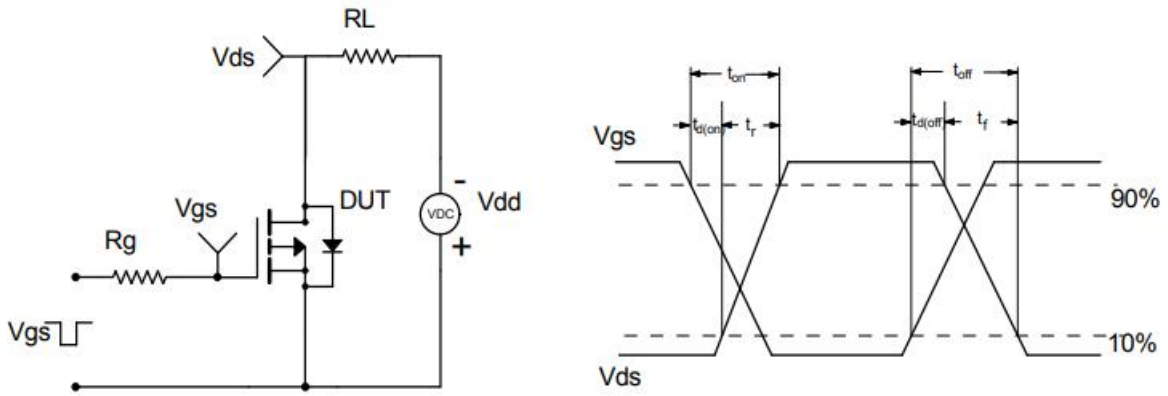


Figure 13. Resistive Switching Test Circuit & Waveforms

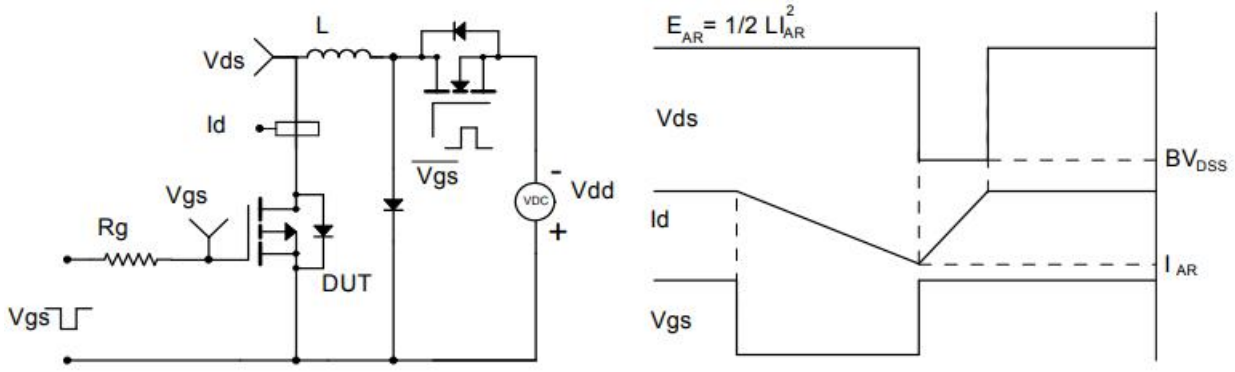


Figure 14. Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

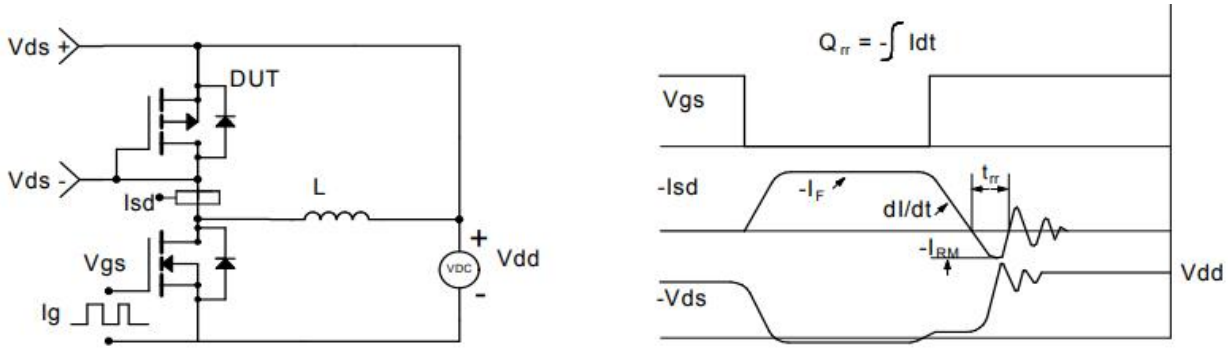
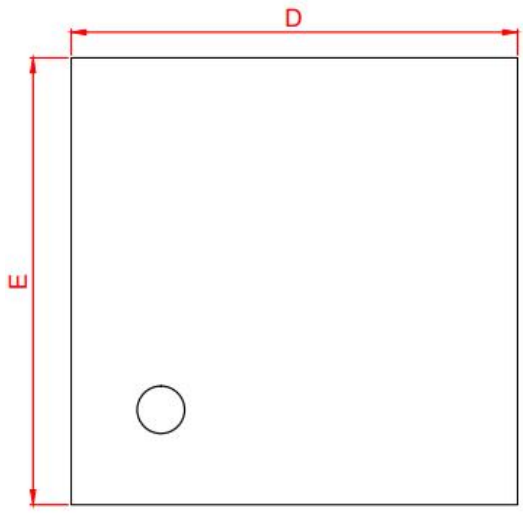
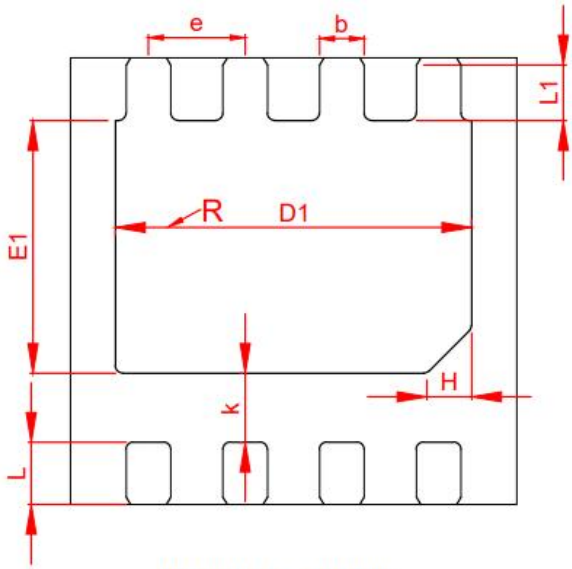


Figure 15. Diode Recovery Test Circuit & Waveforms

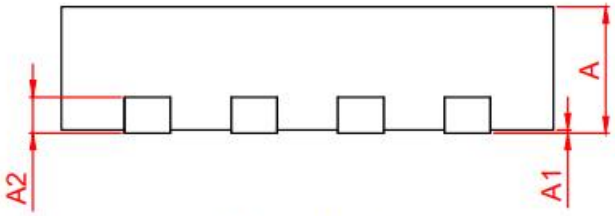
DFN3*3 Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
* A1	0.00	0.02	0.05
* b	0.27	0.32	0.37
* A2	0.20REF		
* D	2.90	3.00	3.10
* E	2.90	3.00	3.10
* E1	1.70	1.80	1.90
* D1	2.35	2.45	2.55
* e	0.65BSC		
* L	0.35	0.40	0.45
h	0.30 REF		
* k	0.50REF		
* L1	0.25	0.30	0.35

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